ICP Family Programmers: FTM Functions

IMPORTANT NOTE: starting from Sep-2016 Softlog Systems manufactures ICP2**(G3)**, ICP2-GANG**(G3)** and ICP2-COMBO**(G3)** programmers additionally to existing ICP2, ICP2-GANG and ICP2-COMBO. Due to nearly full compatibility all of them are referred below as ICP2, ICP2-GANG and ICP2-COMBO respectively. If difference is applied then they are referred as “G3 products” and “non-G3 products”

1 DLL Functions

See files **"c_icpexp.h"** and **"fr_icp2.h"** for detailed description. The relevant functions are listed below:

###	*Function Name*	*Function Description*
1.	Icp2AdConv()	Execute A/D conversion
2.	Icp2DaVolt ()	Set D/A levels (**not** pins) Note: DA_VDD value must be higher than DA_IO
3.	Icp2PinState()	Set/Read pin state
4.	Icp2ClockDataComPar()	Set CLOCK/DATA ("RB6/RB7") communication parameters
5.	Icp2SingleClockDataAction()	Execute single CLOCK/DATA communication
6.	Icp2MultiClockDataAction()	Execute multiple CLOCK/DATA communications
7.	Icp2SafeOff()	Turn ICP pins to safe state (off/inactive)
8.	Icp2SingleClockDataFreq()	Measure period (frequency) at DATA line NOTE: - minimum DLL version: 4.11.1a 11-Mar-13 - minimum firmware version: 18.3

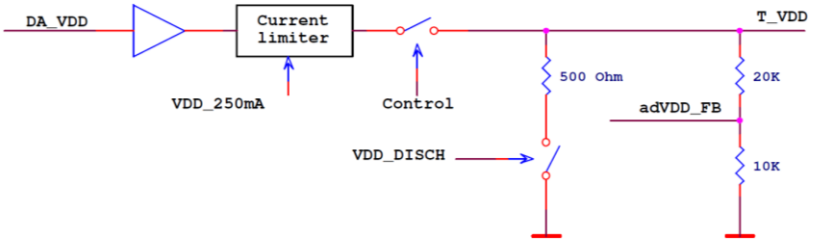
2 Pin Description

IMPORTANT: Settings for pins below will be overridden during ICP programming operation, therefore the desired settings should be **re-applied** after programming is done

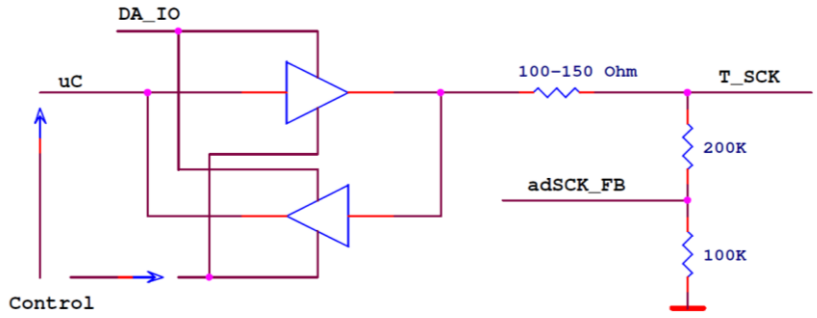
D-type 15 "TARGET" Connector Pin Number	*Pin Name*	*Voltage Level Set by D/A ...*	*High Level Range*	*Operation*	*State after Icp2SafeOff() Function*
1	T_VDD	DA_VDD	2.0...5.5V	VDD output (push only): 0-turn off, 1-turn on, also see VDD_DISCH	Off
2	GND	-	-	-	-
3	T_SCK	DA_IO	2.0...5.5V	I/O type 1: 0-off, 1-on, PIN_Z - tri-state (weak pull-down)	Tri-state
4	T_MOSI	DA_IO	2.0...5.5V	I/O type 1	Tri-state
5	T_MISO	DA_IO	2.0...5.5V	I/O type 1	Tri-state
6	T_VPP	DA_VPP	2.0...13.5V	0-turn off, 1-turn on, PIN_Z - tri-state (weak pull-down)	Tri-state
7	T_TARG	Fixed 5V	5.0V	Output only: 0-off (default), 1-on	Off
8	Non-G3 products: T_VTEST	DA_VPP	2.0...13.5V	Output only: 0-off (default), 1-on	Off
	G3 products: T_DIO_2	DA_IO	2.0...5.5V	I/O type 1	Not affected (default: low output)
9	T_DIO_0	DA_IO	2.0...5.5V	I/O type 1	Tri-state
10	T_DIO_1	DA_IO	2.0...5.5V	I/O type 1	Tri-state
Internal	VDD_DISCH	Internal	Internal	0-disconnect 500Ω from T_VDD 1-connect 500Ω to T_VDD (default)	Not affected
Internal	VDD_250MA	Internal	Internal	0-VDD output current 40mA max 1-VDD output current 250mA max	Not affected
Internal	T_D_SHORT	Internal	Internal	0-disconnect T_MOSI from T_MISO 1-short T_MOSI and T_MISO (default)	Not affected

3 Pin Schematics (Simplified)

3.1 T_VDD



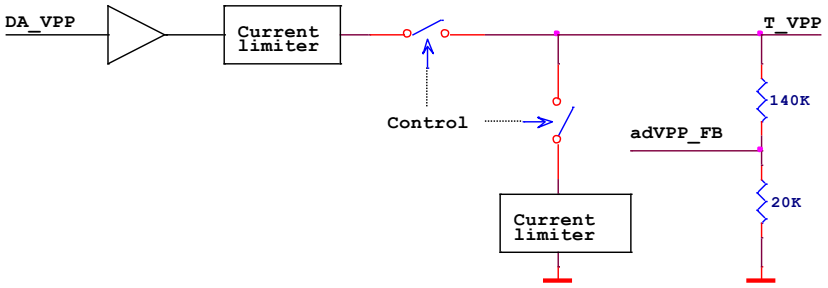
3.2 T_SCK



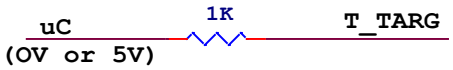
NOTE: resistor 100-150 Ohm is not present in T_SCK and T_MOSI of ICP2(HC)

3.3 T_MOSI, T_MISO, T_DIO_0, T_DIO_1 and T_DIO_2: identical to T_SCK

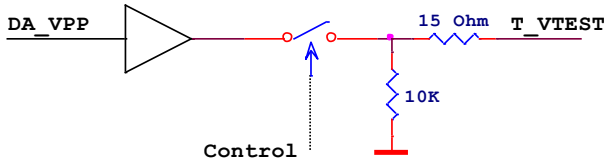
3.4 T_VPP



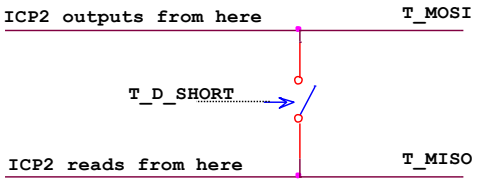
3.5 T_TARG (not available on ICP2-Portable)



3.6 T_VTEST (available on non-G3 products only)



3.7 T_D_SHORT

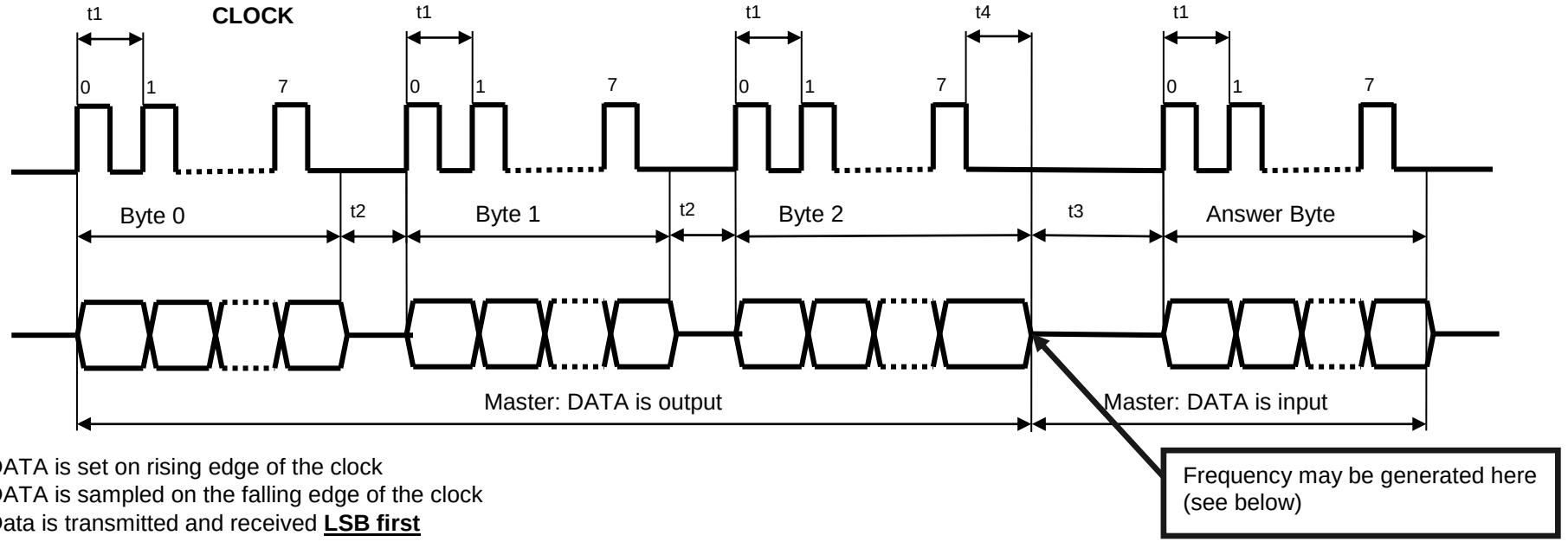


4 CLOCK/DATA ("RB6/RB7") Protocol

4.1 Hardware

Communication is implemented via 2 ICP programming lines: CLOCK (T_SCK) and DATA (T_MOSI/T_MISO). CLOCK is always controlled by ICP (Master), DATA is controlled by MASTER during transmission and by Slave (UUT) during reception of the answer byte

4.2 Waveforms and Timing (from ICP2 point of view)



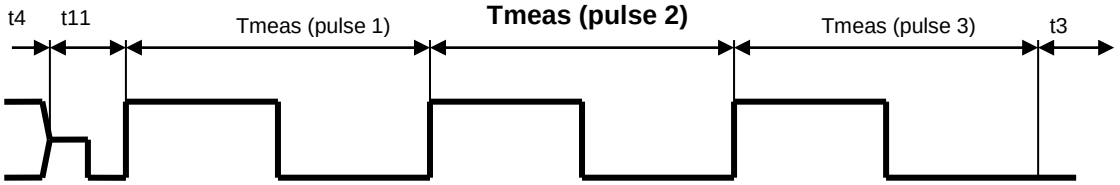
- DATA is set on rising edge of the clock
- DATA is sampled on the falling edge of the clock
- Data is transmitted and received **LSB first**

Parameter	***Description***	***Value***
V_{OL}	CLOCK/DATA low level (no load)	0V
V_{OH}	CLOCK/DATA output high level (no load)	Software programmable: 2.0...5.0V (DA_IO)
V_{IL}	DATA input low level	Maximum $0.2V_{OH}$
V_{IH}	DATA input high level	Minimum $0.8V_{OH}$
t1	Clock period	Software programmable: 2ms (0.5KHz)...0.063ms (16KHz), default: 2ms
t_{CL}	Clock low duration	½ of t1
t_{CH}	Clock high duration	½ of t1
t2	Delay between Master bytes	1 ms for Icp2SingleClockDataAction(), 200us for Icp2MultiClockDataAction()
t3	Delay before answer byte	Software programmable: 1ms…250ms, default: 0ms. NOTE: 5ms is always added after detecting the last falling edge during frequency measurement
t4	Delay between last clock falling edge to data=input	(½ of t1) + 1ms

4.3 Frequency Measurement

Once Icp2SingleClockDataFreq() is received Slave should output 3 pulses at DATA line and then send the usual answer byte. We recommend disabling all interrupts in your firmware during pulse generation for maximum accuracy

Frequency at DATA line generated by Slave



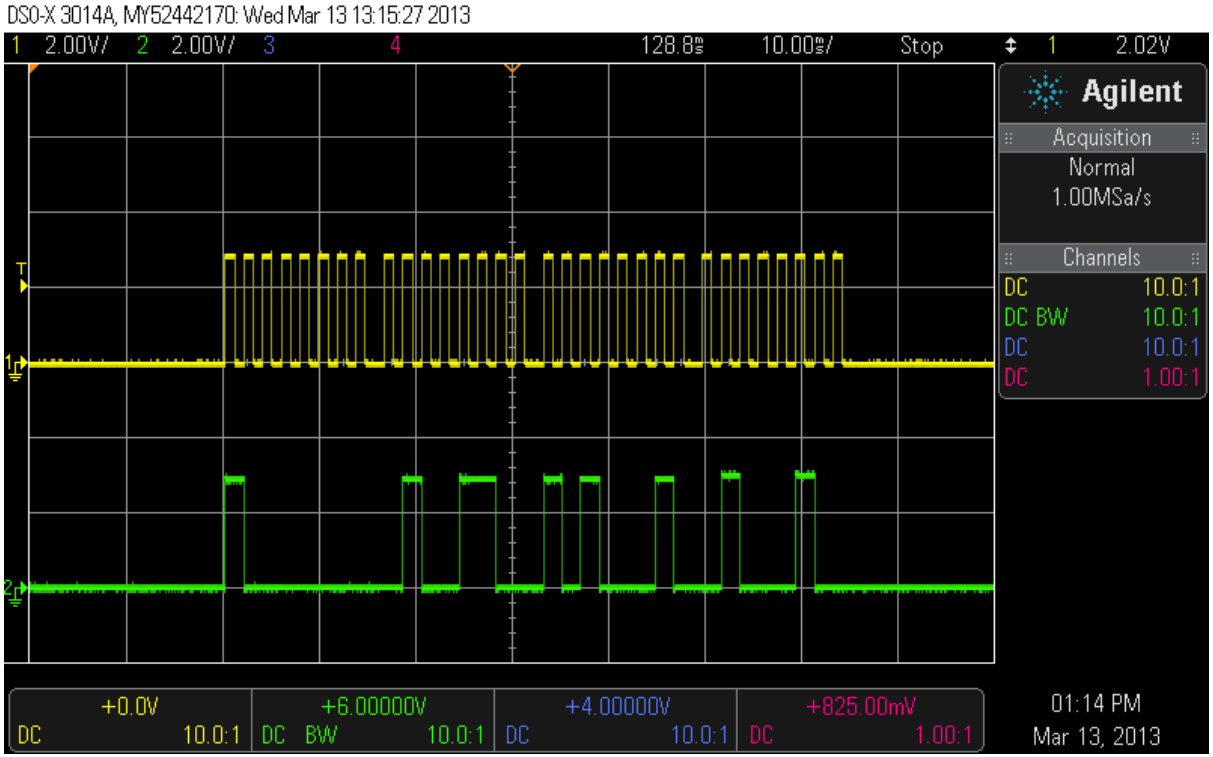
Parameter	***Description***	***Value***
t11	Maximum delay between Master DATA=input and Slave outputs 1st rising edge	5ms (TBD)
Tmeas	Pulse duration. NOTE: ICP2 measures pulse 2 only	1.0…5.0ms (2ms is recommended)
-	Measurement accuracy	≈0.1% for Tmeas≈2ms (Preliminary)

4.4 Sample Waveform: single CLOCK/DATA Communication (Icp2SingleClockDataAction)

4.4.1 Software Sequence

unsigned char answ;
unsigned int period_us;

- Icp2DaVolt (DA_IO, 3000); //preset I/O DAC=3.0V
- Icp2ClockDataComPar(CL_DA_0_5KHZ, 0); //speed 0.5KHz (t1), delay 0ms before answer (t3)
- Icp2SingleClockDataAction (1,0x32,0x45,&answ);



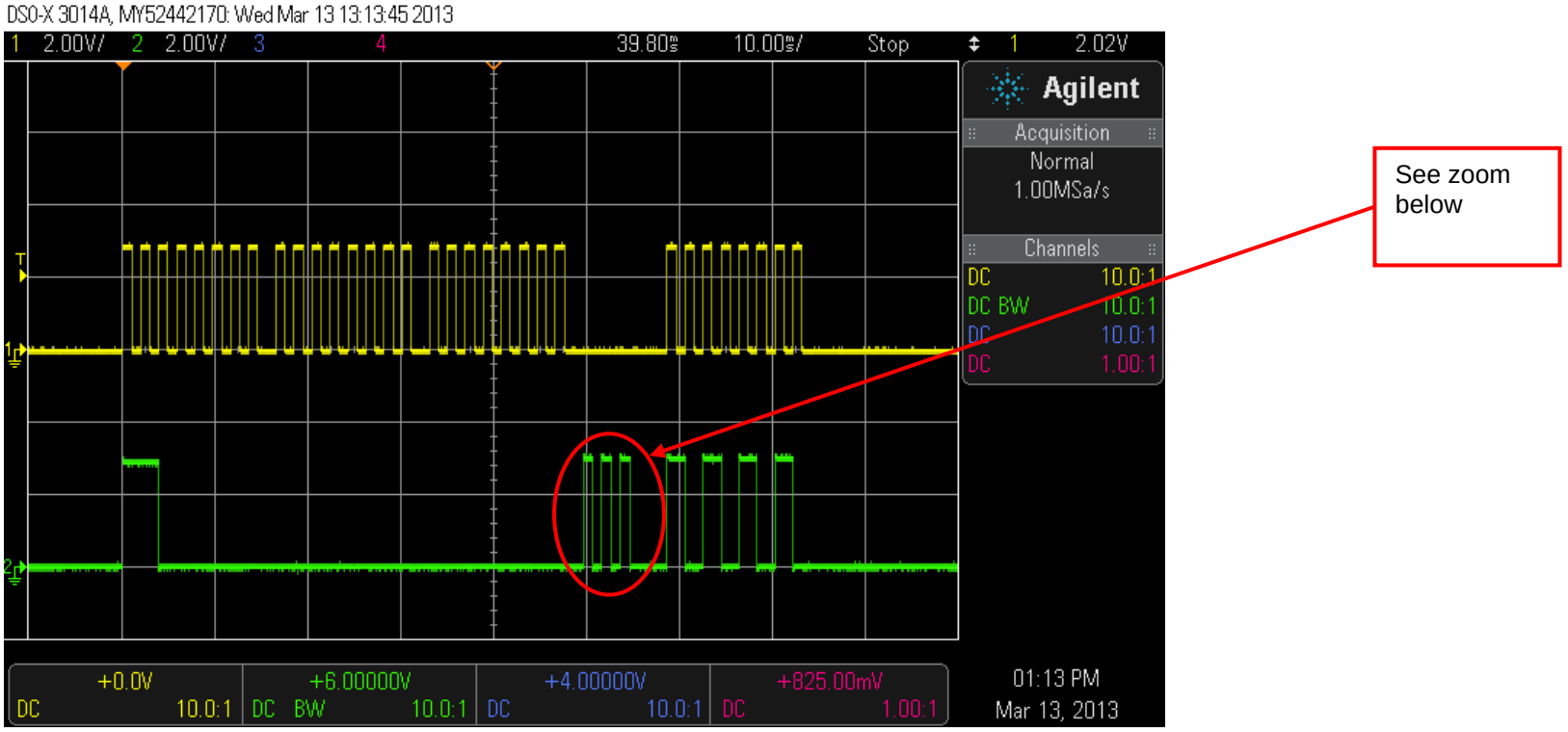
answ = 0x22

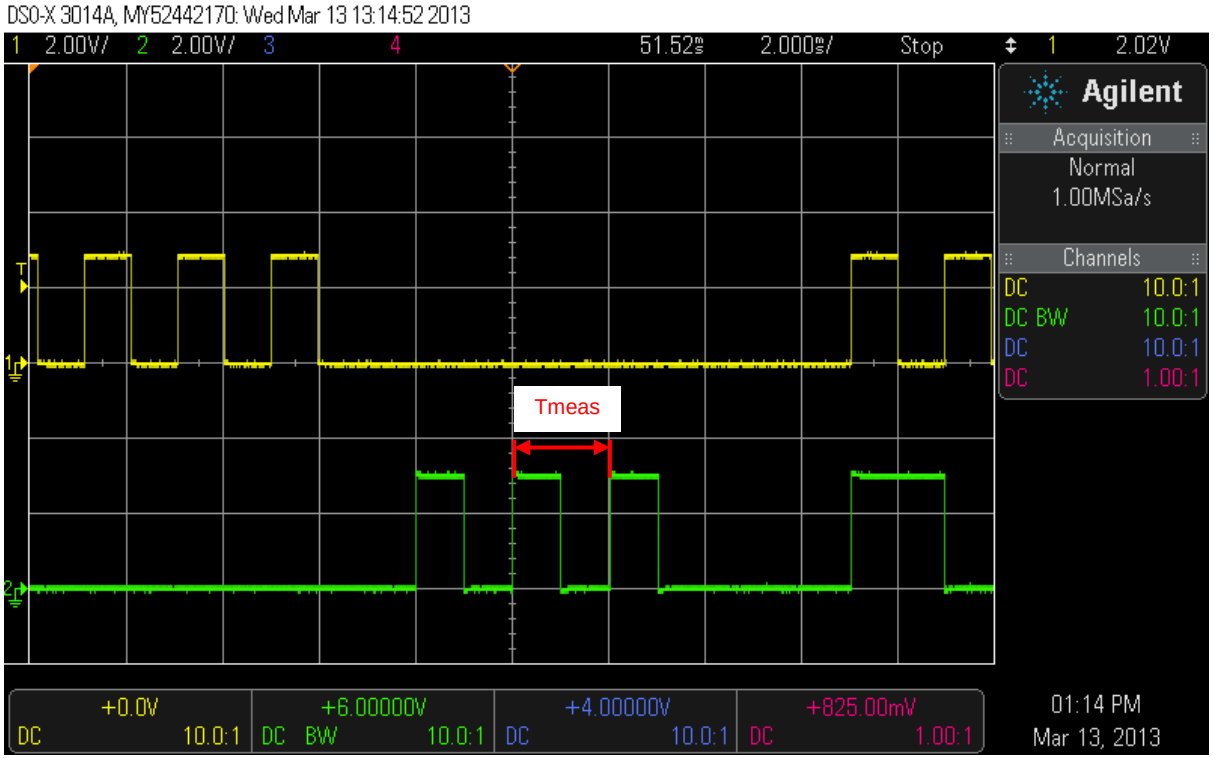
4.5 Sample Waveform: Measure Period (Frequency) at DATA Line (Icp2SingleClockDataFreq)

4.5.1 Software Sequence

unsigned char answ;
unsigned int period_us;

- Icp2DaVolt (DA_IO, 3000); //preset I/O DAC=3.0V
- Icp2ClockDataComPar(CL_DA_0_5KHZ, 0); //speed 0.5KHz (t1), delay 0ms after measurement/before answer (t3)
- Icp2SingleClockDataFreq (3, //Tx byte 0
  0x00, //Tx byte 1
  0x00, //Tx byte 2
  &answ, //pointer to answer byte
  &period_us); //pointer to measured period [us]





period_us = 2014 in this example
answ = 0x55