ICP2(G3), ICP2-GANG(G3), ICP2-Portable(G3) and ICP2-COMBO(G3) Connection Table

ICP2(G3), ICP2-GANG(G3), ICP2-Portable(G3) D-15 Pin No.	ICP2-COMBO(G3) DIN-48 Pin No.	Pin Name	ICSP: PIC10/12/16, PIC18, PIC24, dsPIC,PIC32	I2C	Keeloq®	SPI Flash	Atmel SPI: ATmega, ATtiny	SWD	JTAG	UPDI (ATtiny, ATmega, AVR)	TPI (ATtiny)	PDI (ATxmega)	LPC80x, LPC17xx (UART)
1	B4, B8, B12, B16	T_VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD
2	C2, C3, C6, C7, C10, C11, C14, C15	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
3	A2, A6, A10, A14	T_SCK	CLOCK (PGC)	SCL	CLOCK	SCK	SCK	SWCLK	TCK	-	TPICLK	PDI_CLK	-
4	A3, A7, A11, A15	T_MOSI	DATA (PGD)	SDA	DATA	SI	MOSI	SWDIO	TDI	UPDI	TPIDATA	PDI_DATA	UART0_RX
5	B2, B6, B10, B14	T_MISO	-	-	-	SO	MISO	-	TDO	-	-	-	UART0_TX
6	A1, A5, A9, A13	T_VPP	MCLR/VPP	-	-	-	RESET	RESET (12)	RESET(2)	-	RESET	-	RESET
7	C4, C8, C12, C16	T_TARG	-	-	-	-	-	-	-	-	-	-	-
8	B3, B7, B11, B15	T_DIO_2	-	-	-	CE	-	ERASE (1) ISP entry (3)	TEST (11)	-	-	-	ISP entry (4)
9	A4, A8, A12, A16	T_DIO_0	-	-	-	-	-	-	-	-	-	-	-
10	B1, B5, B9, B13	T_DIO_1	-	-	S1	-	-	-	TMS	-	-	-	-

ICP2(G3), ICP2-GANG(G3), ICP2-Portable(G3) D-15 Pin No.	ICP2-COMBO(G3) DIN-48 Pin No.	Pin Name	Microwire EEPROM (93C46, …)	SWIM (STM8)	SWI (ATSHA204, ATECC608)	BDM (MC9S08)	CYBLE-013025 (UART)	C2 (EFM8)	SBW (MSP430)				
1	B4, B8, B12, B16	T_VDD	VDD	VDD	VCC	VDD	VDD	VDD or VREGIN	VDD				
2	C2, C3, C6, C7, C10, C11, C14, C15	GND	GND	GND	GND	GND	GND	GND	GND				
3	A2, A6, A10, A14	T_SCK	CLK	-	-	-	-	C2CK	SBWTCK				
4	A3, A7, A11, A15	T_MOSI	DI	SWIM (5)	SDA (10)	BKGD (7)	UP_RX (9)	C2D	SBWTDIO				
5	B2, B6, B10, B14	T_MISO	DO	-	-	-	UP_TX	-	-				
6	A1, A5, A9, A13	T_VPP	-	RESET	-	- (8)	XRES (9)	-	-				
7	C4, C8, C12, C16	T_TARG	-	-	-	-	-	-	-				
8	B3, B7, B11, B15	T_DIO_2	CS	-	-	-	SDA (9)	-	-				
9	A4, A8, A12, A16	T_DIO_0	-	-	-	-	-	-	-				
10	B1, B5, B9, B13	T_DIO_1	ORG (6)	-	-	-	-	-	-				

Note 1: Atmel Cortex M7/M4 only (SAM E/S/V, SAM4, SAMG5x)
Note 2: RESET pin is not required for ATmega/ATxmega with JTAG interface
Note 3: ISP entry for LPC80x (recommended)
Note 4: PIO0_12 for LPC80x, P2.10 for LPC17xx – see NXP User's Manuals for details
Note 5: Resistor 1K±10% between SWIM and VDD is required
Note 6: ICP2(G3) family programmers set this pin according to selected memory organization: x8 = GND, x16 = VDD
Note 7: Resistor 2K-10K between BKGD and VDD is recommended
Note 8: No RESET pin connection is required but the RESET pin should have pull-up resistor
Note 9:
- Resistor 2.2K-10K between T_MOSI (D-15 pin 4) and GND (D-15 pin 2) must be connected in order to enter programming mode
- XRES connection with pullup about 10K is recommended for reliable programming
- SDA connection is recommended for possible recovery
Note 10: Resistor 1K between T_MOSI and VDD is required
Note 11: MSP430 only
Note 12: RESET pin is not used for nRF51xxx/nRF528xx devices