

ICP2-COMBO(G3) Production Quality In-Circuit Programmer

Specification

1 Mechanical

ICP2-COMBO(G3) programmer size:

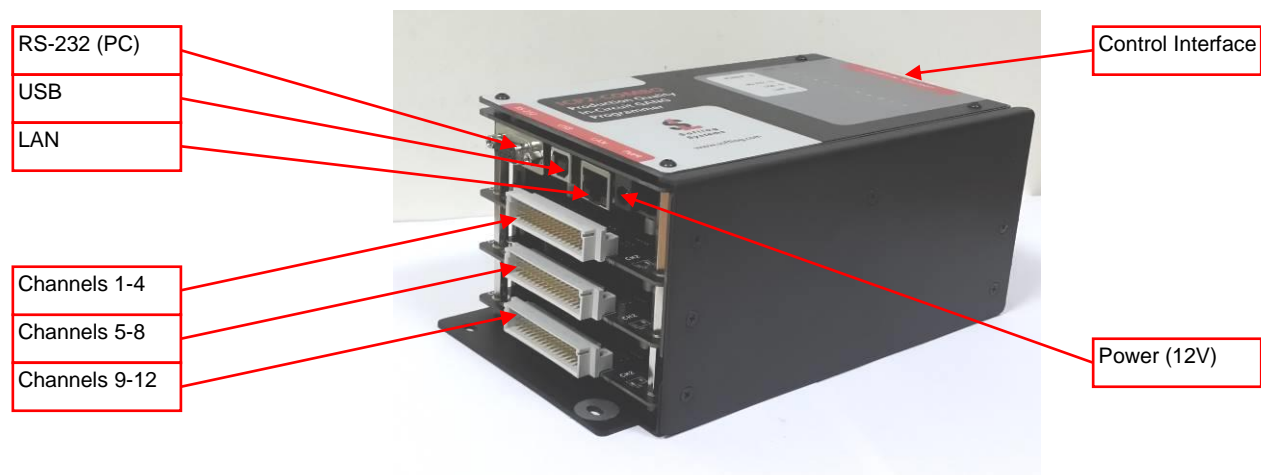
- 12 channels: 215 x 118 x 90 mm
- 8 channels: 215 x 118 x 68 mm
- 4 channels: 215 x 118 x 46 mm

Mounting holes: 4 holes for M3 screws, 200 x 80 mm


2 Connectors

Notes:

- PCB with Channels 9-12 doesn't present on 4-channel and 8-channel versions of ICP2-COMBO(G3)
- PCB with Channels 5-8 doesn't present on 4-channel version of ICP2-COMBO(G3)



2.1 "Power" Connector (Power Jack, Center Pin 2.1mm)

Pin No.	Pin Name	Voltage Range	Pin Type	Description
1/center	POWER (+)	12V to 15V, 5A	Power input with in-series diodes	Main ICP2-COMBO(G3) power supply input 
2	POWER (-)			

2.2 "USB" Connector

Standard USB connector (Type-B Female)

2.3 "LAN" Connector

Standard RJ-45 connector

ICP2-COMBO(G3) Specification

2.4 “RS-232 IN” Connector (D-type 9 Female)

Pin No.	Pin Name	Voltage Range	Pin Type	Description
1	-	-	-	Not connected
2	PC_RXD_ISO	RS-232 level	Standard RS-232 output	TxD output to PC (isolated)
3	PC_TXD_ISO	RS-232 level	Standard RS-232 input	RxD input from PC (isolated)
4	-	-	-	Not connected
5	GND_ISO	-	Isolated GND	Ground connection (isolated)
6,7,8,9	-	-	-	Not connected

2.5 “TARGET” Connector (DIN-48, A, B, C, male), 3 Identical Connectors

Mating connector: 86093488314755V1LF (FCI) - DIN41612, 3 rows, 48 pins, female, C/2 style, straight

Pin Number				Pin Name	Opto-relay barrier	Pin Type	Description
CH. 1 CH. 5 CH. 9	CH. 2 CH. 6 CH. 10	CH. 3 CH. 7 CH. 11	CH. 4 CH. 8 CH. 12				
A1	A5	A9	A13	T_VPP/ MCLR	Yes	Power output or input with weak pull-down	Target VPP/MCLR supply voltage
A2	A6	A10	A14	T_SCK	Yes	CMOS output or input with weak pull-down and programmable pull-up and pull-down	Target clock
A3	A7	A11	A15	T_MOSI	Yes	CMOS output or input with weak pull-down and programmable pull-up and pull-down	Target data
A4	A8	A12	A16	T_DIO_0	Yes	CMOS output or input with weak pull-down	Target I/O number 0
B1	B5	B9	B13	T_DIO_1	Yes	CMOS output or input with weak pull-down	Target I/O number 1
B2	B6	B10	B14	T_MISO	Yes	CMOS output or input with weak pull-down and programmable pull-up and pull-down	Target data, internally connected to T_MOSI
B3	B7	B11	B15	T_DIO_2	Yes	CMOS output or input with weak pull-down	Target I/O number 2
B4	B8	B12	B16	T_VDD	Yes	Power output or input with weak pull-down and programmable strong pull-down	Target VDD supply voltage
C1	C5	C9	C13	GND_SW	Yes	-	Ground connection via opto-relay barrier. Not recommended
C2, C3	C6, C7	C10, C11	C14, C15	GND	-	-	Ground connection (permanent)
C4	C8	C12	C16	T_TARG	-	CMOS output	General purpose output

ICP2-COMBO(G3) Specification

2.6 “Control Interface” Connector (DIN-64, A, B, male)

Mating connector: 09022646421 (Harting) - DIN41612, 2 rows, 64 pins, female, B style, receptacle, straight

NOTE: all voltages are referred to isolated GND (GND_ISO)

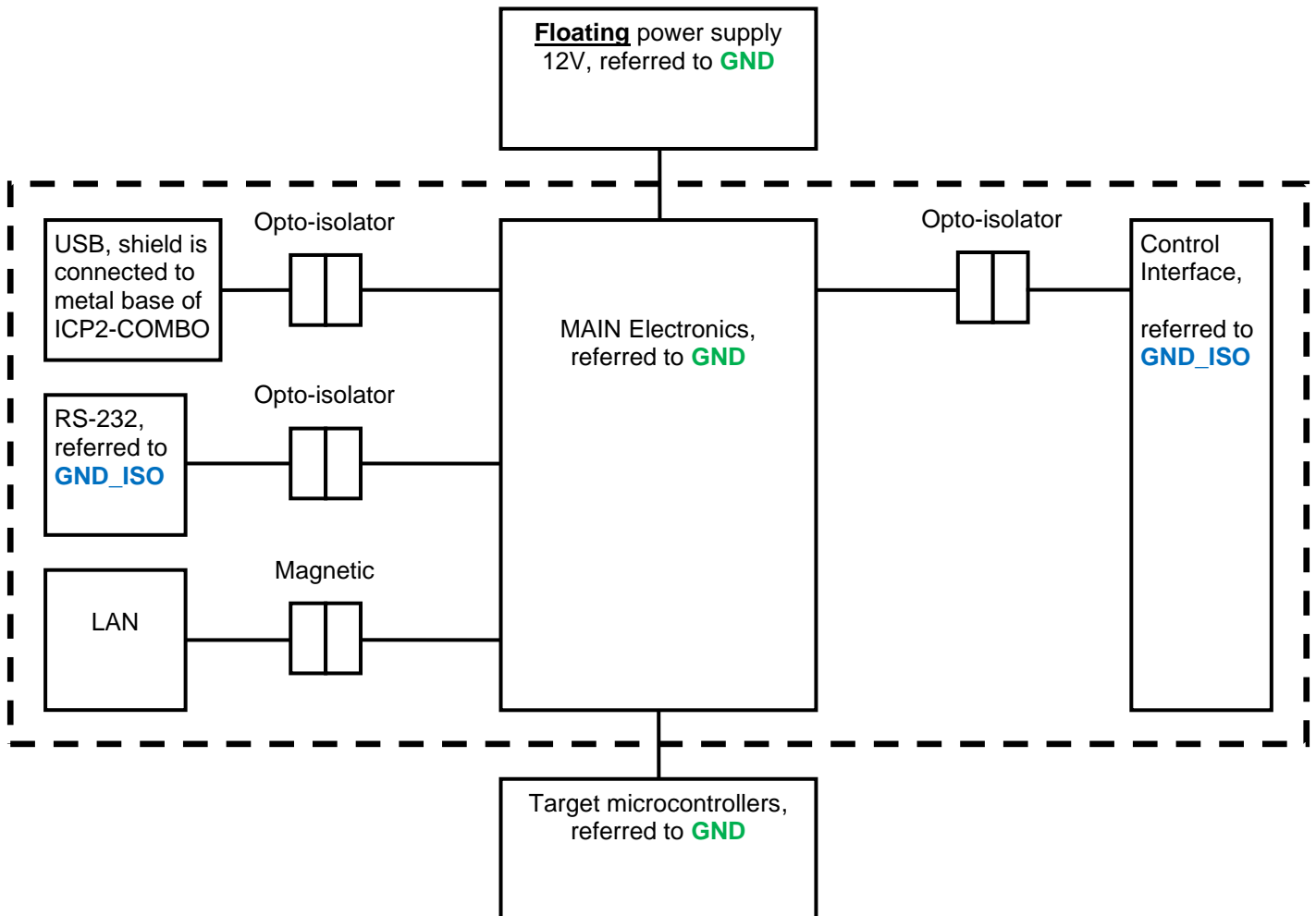
Pin No.	Pin Name	Pin Type	Description
A1	-		
B1	5V_ISO	5V reference source	Isolated 5V with in-series fuse 50mA, can be used to control ENV_SEL_A/B/C_ISO lines
A2	GND_ISO	-	Isolated GND
B2	GND_ISO	-	Isolated GND
A3	PC_RXD_ISO	Standard RS-232 output	RS-232 output to PC
B3	PC_TXD_ISO	Standard RS-232 input	RS-232 input from PC
A4	CHAIN_232_RXD_ISO	Standard RS-232 input	RS-232 input from chained ICP2-COMBO(G3)
B4	CHAIN_232_TXD_ISO	Standard RS-232 output	RS-232 output to chained ICP2-COMBO(G3)
A5	GND_ISO	-	Isolated GND
B5	GND_ISO	-	Isolated GND
A6	ENV_SEL_A_ISO	CMOS input (0/5V) with weak pull-down	Environment selection (bit 0)
B6	ENV_SEL_B_ISO	CMOS input (0/5V) with weak pull-down	Environment selection (bit 1)
A7	ENV_SEL_C_ISO	CMOS input (0/5V) with weak pull-down	Environment selection (bit 2)
B7	-	-	-
A8	-	-	-
B8	GND_ISO	-	Isolated GND
A9	GO_ISO_1	CMOS input (0/Z) with weak pull-up	Ch. 1: programming activation (active low)
B9	GO_ISO_2	CMOS input (0/Z) with weak pull-up	Ch. 2: programming activation (active low)
A10	GO_ISO_3	CMOS input (0/Z) with weak pull-up	Ch. 3: programming activation (active low)
B10	GO_ISO_4	CMOS input (0/Z) with weak pull-up	Ch. 4: programming activation (active low)
A11	GO_ISO_5	CMOS input (0/Z) with weak pull-up	Ch. 5: programming activation (active low)
B11	GO_ISO_6	CMOS input (0/Z) with weak pull-up	Ch. 6: programming activation (active low)
A12	GO_ISO_7	CMOS input (0/Z) with weak pull-up	Ch. 7: programming activation (active low)
B12	GO_ISO_8	CMOS input (0/Z) with weak pull-up	Ch. 8: programming activation (active low)
A13	GO_ISO_9	CMOS input (0/Z) with weak pull-up	Ch. 9: programming activation (active low)
B13	GO_ISO_10	CMOS input (0/Z) with weak pull-up	Ch. 10: programming activation (active low)
A14	GO_ISO_11	CMOS input (0/Z) with weak pull-up	Ch. 11: programming activation (active low)
B14	GO_ISO_12	CMOS input (0/Z) with weak pull-up	Ch. 12: programming activation (active low)
A15	-	-	-
B15	-	-	-
A16	-	-	-
B16	-	-	-
A17	PASS_ISO_1	CMOS output with in-series R=330Ω	Ch. 1: pass/busy indication
B17	PASS_ISO_2	CMOS output with in-series R=330Ω	Ch. 2: pass/busy indication
A18	PASS_ISO_3	CMOS output with in-series R=330Ω	Ch. 3: pass/busy indication
B18	PASS_ISO_4	CMOS output with in-series R=330Ω	Ch. 4: pass/busy indication
A19	PASS_ISO_5	CMOS output with in-series R=330Ω	Ch. 5: pass/busy indication
B19	PASS_ISO_6	CMOS output with in-series R=330Ω	Ch. 6: pass/busy indication
A20	PASS_ISO_7	CMOS output with in-series R=330Ω	Ch. 7: pass/busy indication
B20	PASS_ISO_8	CMOS output with in-series R=330Ω	Ch. 8: pass/busy indication
A21	PASS_ISO_9	CMOS output with in-series R=330Ω	Ch. 9: pass/busy indication
B21	PASS_ISO_10	CMOS output with in-series R=330Ω	Ch. 10: pass/busy indication
A22	PASS_ISO_11	CMOS output with in-series R=330Ω	Ch. 11: pass/busy indication
B22	PASS_ISO_12	CMOS output with in-series R=330Ω	Ch. 12: pass/busy indication
A23	-	-	-
B23	-	-	-
A24	-	-	-
B24	-	-	-
A25	FAIL_ISO_1	CMOS output with in-series R=330Ω	Ch. 1: fail/busy indication
B25	FAIL_ISO_2	CMOS output with in-series R=330Ω	Ch. 2: fail/busy indication
A26	FAIL_ISO_3	CMOS output with in-series R=330Ω	Ch. 3: fail/busy indication
B26	FAIL_ISO_4	CMOS output with in-series R=330Ω	Ch. 4: fail/busy indication
A27	FAIL_ISO_5	CMOS output with in-series R=330Ω	Ch. 5: fail/busy indication
B27	FAIL_ISO_6	CMOS output with in-series R=330Ω	Ch. 6: fail/busy indication
A28	FAIL_ISO_7	CMOS output with in-series R=330Ω	Ch. 7: fail/busy indication
B28	FAIL_ISO_8	CMOS output with in-series R=330Ω	Ch. 8: fail/busy indication
A29	FAIL_ISO_9	CMOS output with in-series R=330Ω	Ch. 9: fail/busy indication
B29	FAIL_ISO_10	CMOS output with in-series R=330Ω	Ch. 10: fail/busy indication
A30	FAIL_ISO_11	CMOS output with in-series R=330Ω	Ch. 11: fail/busy indication
B30	FAIL_ISO_12	CMOS output with in-series R=330Ω	Ch. 12: fail/busy indication
A31	-	-	-
B31	-	-	-
A32	-	-	-
B32	-	-	-

ICP2-COMBO(G3) Specification

3 Environment Selection (0=GND_ISO, 1=5V_ISO)

<i>ENV_SEL_C_ISO</i>	<i>ENV_SEL_B_ISO</i>	<i>ENV_SEL_A_ISO</i>	<i>Environment Number</i>
Not connected	Not connected	Not connected	1
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	Reserved, selects 1
1	1	1	Reserved, selects 1

4 Ground Domains



5 Opto-Relay Barrier

Every ICP2-COMBO(G3) channel features **built-in** opto-relay barrier which may disconnect programming lines from the target after programming/verification is done. See opto-relay parameters below.

Note: T_VDD and T_VPP lines contain high-current 60V opto-relays (SSR). For further protection external varistors are recommended on T_VDD and T_VPP as follows (P/N example): **V05E14P** (Littelfuse)

ICP2-COMBO(G3) Specification

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

WARNING: ventilation (fan) is required if ICP2-COMBO(G3) is placed into closed equipment

Symbol	Parameter	Min.	Max.	Unit
T _{ST}	Storage temperature	-30	+80	°C
T _A	Operating temperature (ventilation is required)	0	+50	°C
V _{IN}	Input supply voltage	-18	18	V
I _{IN}	Input supply current	0	5	A
V _{RS}	RS-232 voltage	-15	15	V
V _{DD}	T_VDD voltage	-10	10	V
V _{PP}	T_VPP/MCLR voltage	-10	20	V
V _{PRG}	T_SCK, T_MOSI, T_MISO, T_DIO_0, T_DIO_1 and T_DIO_2 voltage	-7.5	7.5	V
V _{TARG}	T_TARG voltage	-7.5	7.5	V
V _{GO}	GO_ISO voltage (referred to GND_ISO)	- 10	10	V
V _{PF}	PASS_ISO and FAIL_ISO voltage (referred to GND_ISO)	- 6.5	6.5	V
V _{GND-GNDISO}	Galvanic isolation between Control/RS-232 Interface and GND	TBD	TBD	kV
V _{GND-USB}	Galvanic isolation between USB and GND	TBD	TBD	kV
V _{OPTORELAY}	Blocking voltage between GND and target (opto-relay barrier)	50	50	V

6.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
T _A	Operating temperature	0	+50	°C
V _{IN}	Input supply voltage	11	15	V
-	T_VDD current	-	200	mA
-	T_VPP/MCLR resistive load to GND or T_VDD	1	-	KΩ
-	T_VPP/MCLR capacitive load to GND	-	22	nF
-	T_SCK, T_MOSI, T_MISO, T_DIO_0, T_DIO_1 and T_DIO_2 resistive load to GND or T_VDD	1	-	KΩ
-	T_SCK, T_MOSI, T_MISO, T_DIO_0, T_DIO_1 and T_DIO_2 capacitive load to GND or T_VDD	-	33	pF

ICP2-COMBO(G3) Specification

6.3 On-Board Flash Memory (Per Channel)

(TA = 0 to 50°C, unless otherwise specified. Typical values are referred to TA = 25°C)

Param No.	Parameter	Test Condition	Min.	Typ.	Max.	Unit
M001	Capacity	All conditions	-	32	-	MByte
M002	Endurance	All conditions	10K	100K	-	-
M003	Data retention	All conditions	20	-	-	Years
M004	Logical number of environments	All conditions	-	6	-	-

6.4 On-Board EEPROM (Per Channel)

(TA = 0 to 50°C, unless otherwise specified. Typical values are referred to TA = 25°C)

Param No.	Parameter	Test Condition	Min.	Typ.	Max.	Unit
E001	Secure non-volatile counter endurance	All conditions	8M	-	-	-
E002	Data retention	All conditions	40	-	-	Years

6.5 DC Characteristics

(TA = 0 to 50°C, unless otherwise specified. Typical values are referred to TA = 25°C)

Param No.	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Input Voltage					
D001	Input supply voltage	All conditions	11	-	15	V
D002	Input supply current	V _{IN} =12V, no operation, 12 channel, all opto-relays are on	-	910	-	mA
	T_VDD Input/Output (Per Channel)					
D010	Output high level	ICP powered mode	1.8	-	5.5	V
	Input high level	Target powered mode	1.8	-	6.0	V
D011	Current limit (short to GND)	V _{IN} =12V to 15V	250	300	-	mA
D013	Weak pull-down resistor	All conditions	-	30	-	KΩ
D014	Programmable strong pull-down resistor	All conditions	-	500	-	Ω
D015	Opto-relay leakage current	All conditions	-	0.003	1.0	uA
	T_VPP/MCLR Output (Per Channel)					
D020	Output high level	All conditions	1.8	-	13.5	V
D021	Current limit (short to GND) Note: higher current is available – contact Softlog	All conditions	30	-	-	mA
D022	Weak pull-down resistor	All conditions	-	160	-	KΩ
D023	Opto-relay leakage current	All conditions	-	0.003	1.0	uA
	Programming I/Os (Per Channel): T_SCK, T_MOSI, T_MISO, T_DIO_0,					

ICP2-COMBO(G3) Specification

Param No.	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	T_DIO_1, T_DIO_2					
D040	Output/input high level	All conditions	1.8	-	5.5	V
D041	Output impedance	All conditions	-	120 (Note 1)	-	Ω
D042	Weak pull-down resistor	All conditions	-	300	-	K Ω
D043	Opto-relay leakage current	All conditions	-	0.001	1.0	μ A
	GO Input (Per Channel)					
D050	Input low level	All conditions	0	-	0.8	V
D051	Pull-up resistor	All conditions	-	10	-	K Ω
D052	Input high level	All conditions	4.0	-	5.0	V
	PASS and FAIL Outputs (Per Channel)					
D060	Output impedance	All conditions	-	330	-	Ω
D061	Output low level	No load	-	-	0.2	V
D062	Output high level	No load	4.8	-	-	V
	V_TARG Output (Per Channel)					
D070	Output impedance	All conditions	-	1	-	K Ω
D071	Output low level	No load	-	-	0.2	V
D072	Output high level	No load	4.8	-	-	V
	ENVIRONMENT Select Inputs					
D080	Input low level	All conditions	0	-	0.8	V
D081	Pull-down resistor	All conditions	-	100	-	K Ω
D082	Input high level	All conditions	4.0	-	5.0	V

Note 1: 20 Ω are added due to opto-relay barrier

ICP2-COMBO(G3) Specification

6.6 AC Characteristics

(TA = 0 to 50°C, unless otherwise specified. Typical values are referred to TA = 25°C)

Param No.	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	T_VDD Output					
A001	Rise time	V _{IN} =12V, V _{dd} =5.0V, no load	-	0.07	-	ms
A002	Fall time	V _{IN} =12V, V _{dd} =5.0V, no load	-	2	-	ms
A003	Rise time	V _{IN} =12V, V _{dd} =5.0V, C _{load} =100uF	-	1.5	-	ms
A004	Fall time	V _{IN} =12V, V _{dd} =5.0V, C _{load} =100uF	-	200	-	ms
A005	Rise time	V _{IN} =12V, V _{dd} =5.0V, C _{load} =1000uF, R _{load} =22Ω	-	20	-	ms
A006	Fall time	V _{IN} =12V, V _{dd} =5.0V, C _{load} =1000uF, R _{load} =22Ω	-	50	-	ms
	T_VPP/MCLR Output					
A010	Rise time	V _{IN} =12V, V _{pp} =13V, no load	-	0.1	-	us
A011	Fall time	V _{IN} =12V, V _{pp} =13V, no load	-	0.4	-	us
A012	Rise time to 0V to 10V	V _{IN} =12V, V _{pp} =13V, C _{load} =33nF	-	0.7	-	us
A013	Fall time from 13V to 1V	V _{IN} =12V, V _{pp} =13V, C _{load} =33nF	-	3	-	us
	Programming I/Os: T_SCK, T_MOSI, T_MISO, T_DIO_0, T_DIO_1, T_DIO_2					
A030	Rise time	V _{dd} =5V, no load	-	10	-	ns
A031	Fall time	V _{dd} =5V, no load	-	10	-	ns
A032	T_SCK frequency	All conditions	-	-	10	MHz
A032	T_SCK programmable frequencies	All conditions	-	0.5, 0.625, 0.714, 0.833, 1.0, 1.25, 1.67, 2.5, 5.0, 10.0	-	MHz

7 Revision History

- Feb-24: minimum supply voltage reduced to 11V (old: 12V)
- Nov-21:
 - removed "typical connection" table
 - added environment selection table
 - added recommendation for using varistors on T_VDD and T_VPP lines
- Jan-20 – minor changes:
 - updated typical connection table
 - added recommendation for ventilation (fan)
- Mar-17: initial revision of this document

Information furnished is believed to be accurate and reliable. However, Softlog Systems assumes no responsibility for the consequences of use of such information or for any infringement of patents or other rights of third parties which may result from its use. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied.

© 2024 Softlog Systems (2006) Ltd. - All Rights Reserved